Progress Towards Prolonged IC Deployment Into Previously Inaccessible Hostile Environments Via Development of SiC JFET-R ICs

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Abstract

This invited plenary paper summarizes recent significant progress towards development and deployment of manufacturable SiC JFET-R ICs technology for beneficial prolonged use in extreme environmental conditions previously inaccessible to semiconductor electronics.

INTRODUCTION

Substantial expansion of the practical environmental envelope for integrated circuit (IC) operation offers important benefits to a variety of automotive, aerospace, deep-well drilling, and manufacturing applications [1]. For the majority of these applications, ICs that can reliably operate for long time periods (years) in a harsh environment without degradation or need of diagnostic/maintenance intervention enable the largest benefits compared to IC technologies requiring added shielding, cooling, remote-location, maintenance, or other overhead in order to perform beneficial system functions. The ability to "cold-start" at low temperature (T ≤ -55 °C), continuously function through "warm-up" to reliably function at extremely high temperature (T ≥ 500 °C) through many operational cycles over years would enable significant advancements in aerospace systems including jet engines.

DESIGN FOR HIGH-T DURABILITY

As premature failure of any weakest link would invalidate desired application benefits, a robust chain of "over-designed" technologies were developed and implemented with the overriding goal of establishing application-viable stable and prolonged operation in the most challenging environment of 500 °C air-ambient that is far beyond existing silicon and silicon-on-insulator (SOI) IC capability. In the drive to achieve 500 °C durability, other common IC performance metrics (such as high-frequency operation) were relegated to lesser priority. Key links in this durable technology chain include:

1) 4H-SiC: Among the most chemically inert of the wide band gap semiconductors, which enables dopants and interfaces to remain fixed/stable over long 500 °C operating times. Defects and thermal expansion mismatch stress present in heteroepitaxial semiconductor device systems are importantly avoided given the larger temperature span. Furthermore, there is well-established 4H-SiC wafer, homoepilayer, and power diode/transistor mass-production infrastructure that can be leveraged into manufacturing of extreme-environment ICs.

2) N-channel JFETs and resistors: The integrated device structure of Fig. 1 features inherently robust SiC pn-junctions and is thus not subject to high-T gate-oxide degradation mechanisms that preclude long-term 500 °C durability from being realized in SiC MOSFETs. Compared to SiC BJT, SiC n-JFET is far less sensitive to p-type ohmic contact resistance. Epitaxial pn junctions structurally minimize high-T leakage currents along with negative signal voltage circuit architecture that avoids forward-biasing these pn-junctions. The JFETs are depletion mode, with negative threshold voltage V_T exclusively determined by the as-grown SiC homoepilayers, which to date have exhibited a systematic thickness dependence upon distance from the SiC wafer center [3].

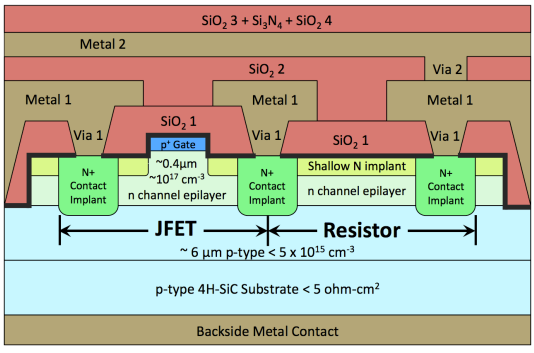

Fig. 1. Simplified cross-sectional illustration of NASA Glenn 4H-SiC JFET-R integrated device approach with two levels of interconnect [2]. The implementation of JFET and Resistor in 4H-SiC facilitates straightforward circuit design and operation over wide temperature range.

3) Layout ratio circuit design: Since JFET and resistor conductance is governed by the same 4H-SiC n-channel in Fig. 1, the temperature compensation of circuits is effectively built-in to the JFET-R IC approach as evidenced in Fig. 2 [2-5]. Circuit design is therefore specified using component dimensional layout ratios instead of T-dependent current/resistance values that can change roughly 400% between 25 °C and 500 °C. The logic gate power also changes correspondingly with temperature (e.g., from ~ 8 mW at 25 °C to ~ 2 mW at 460 °C for the Gen. 11 "Base Power" gate design). The circuit topology requires $+V_{DD}$ and $-V_{SS}$ power supplies and the signal voltages are designed negative with respect to GND. As evidenced in Fig. 2 measured data, this layout ratio topology accommodates both wafer position V_T variation and T dependence.

4) Two-level 500 °C durable interconnect: The two interconnect levels enable increased circuit densities to be realized over single-level interconnect designs. Details regarding the two-level interconnect implementation and its manufacturing requirements are described in a separate invited paper at this conference [6].

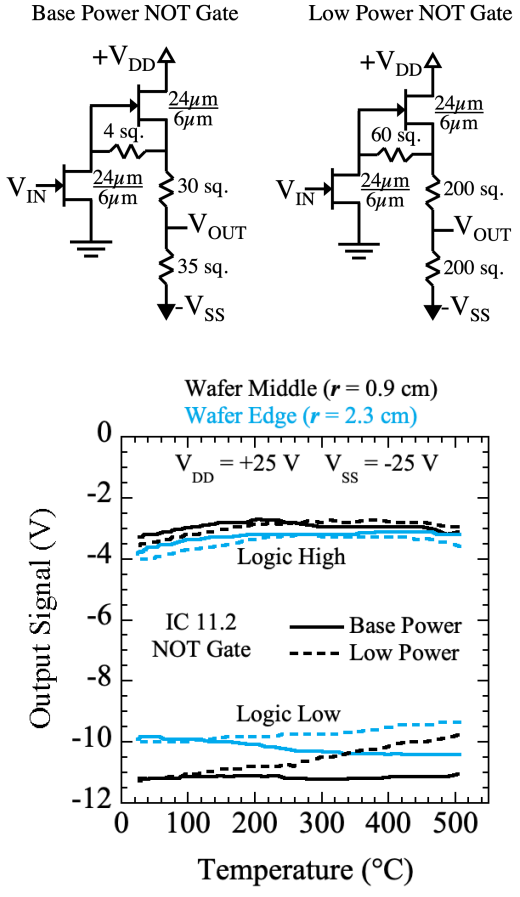

Fig. 2. SiC JFET-R logic based on shared FET/resistor n-channel and dimensional ratio design (top, schematics) enables in built-in temperature compensation (bottom, measured Gen. 11 results) [5].

5) Bond pads: Specialized "IrIS" metal stack anchored directly to SiC around the chip periphery to support gold ball wire bonds will also be described in more detail elsewhere at this conference [6].

6) Ceramic packaging and multi-chip circuit boards: Fig. 3 shows a 4-layer ceramic circuit board with SiC ICs under preparation for upcoming Venus chamber functional test. The packages and boards are implemented using custom-designed but commercially manufactured High Temperature Cofired Ceramic (HTCC) alumina packages and circuit boards with co-fired platinum conductive traces. Gold die attach is employed as described in [7]. It is worth noting that since the chips themselves withstand extremely harsh environments, the packages need not to be hermetically sealed. The attached gold wires seen in Fig. 3 will connect to nearby boards inside the chamber as well as to high-T/high-P chamber-wall feedthroughs leading to test instruments outside the chamber.

Extreme Environment Results

Analog and digital SiC JFET-R circuits have been prototyped and tested in extreme environments. The following summarizes the pioneering results obtained during testing of various ICs fabricated during the NASA Glenn "Generation 10" prototype wafer run:

1) -190 °C to +812 °C operation: This 1022 °C temperature span was demonstrated for logic circuits without any adjustments to input voltages (Fig. 4) [4]. It is also worth noting that an 11-stage ring oscillator achieved very brief +961 °C operation [8].
2) 1 year of stable 500 °C operation: ICs approaching 200 transistors/chip were electrically operated for over 1 year

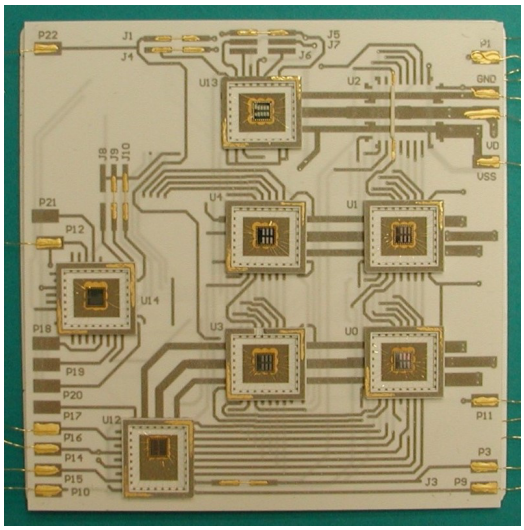

Fig. 3. Photo of 11 cm x 11 cm prototype ceramic circuit board with packaged Gen. 11 SiC JFET-R chips (prior to attaching lids) in preparation for upcoming 460 °C, 91 atmosphere Venus chamber testing [5].

in 500 °C air-ambient ovens with negligible change in circuit characteristics. 500 °C oven-testing was ended prior to all ICs failing [2].

3) Total Ionizing Dose (TID) Radiation: Gen. 10 JFET-R ICs successfully withstood 7 Mrad(Si) TID at 25 °C without any observed device failures [9]. While additional TID testing is needed to reach the TID limits of NASA Glenn SiC JFET-R ICs, prior TID studies of other SiC JFETs indicates TID immunity in excess of 100 Mrad(Si) dose levels might be obtained [10].
4) Single-Event Heavy Ion Strike Radiation: Gen. 10 ICs were tested through linear energy transfer (LET) of 86 MeV-cm^2/mg at 25 °C under electrical bias, and no destructive failure was observed. Soft errors were observed on some devices starting at LET of 3.5 MeV-cm^2/mg, but regenerative flip flops exhibited no such errors through 86 MeV-cm^2/mg LET [9].
5) Venus surface environment: Gen. 10 JFET-R ICs operated unprotected in 9.3 MPa 460 °C chemically caustic Venus surface environment in test chamber for 60 days without failure. The 60 days was limited by Venus test chamber availability, not the SiC ICs [11].

The number of chips subjected to each test was less than 10, and a few cases of "infant 500 °C fail" (< 2000 hours) were observed [2]. Laboratory upgrades are presently underway towards achieving greatly improved testing statistics for T ≥ 500 °C and additionally facilitate more rapid repetitive thermal cycling. Even under limited statistics, cracking of dielectric layers leading to oxidation of underlying interconnect metals has been elucidated as the clearly dominant mechanism limiting long-term high-temperature IC durability [12].

As seen in Table I, Gen. 11 ICs implemented roughly 5-fold more complex ICs than Gen. 10. This increased complexity enabled recent 500 °C demonstrations of 8-bit analog to digital converter IC as well as ~1 kbit read only memory IC (Fig. 4), among a number of other relevant capabilities including the application specific ICs (ASICs) for the Venus mission circuit board depicted in Fig. 3 [5,13]. However, the Gen. 11 interconnect process, which was altered from Gen. 10 in effort to mitigate dielectric cracking as well as enable larger die size, resulted in metal peeling near the wafer periphery, degraded dielectric cracking properties, and subsequently inferior circuit yields [14]. In contrast to yearlong 500 °C durability achieved in Gen. 10, no Gen. 11 chips oven-tested to date have reached 1000 hours of 500 °C operation without malfunction. Therefore, presently on-going development of improved interconnect/dielectric is paramount to successful realization of 500 °C durable Gen. 12 prototype ICs.

Progress Towards Manufacturing

With the initial technical foundation of greatly expanded environmental envelope established, present work beyond further interconnect optimization includes upscaling chip-complexity in parallel with lowering barriers to manufacturability and application infusion. Table I shows progress in relevant IC benchmarks for the most-recent successive developmental prototype generations of NASA Glenn JFET-R chips.

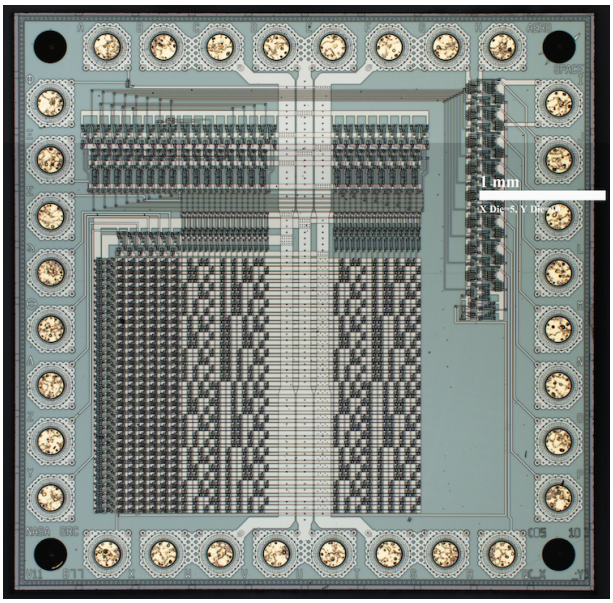

Fig. 4. Photo of 4.65 mm x 4.65 mm 992-bit IC Version 11.3 read-only memory chip prior to packaging and testing at 500 °C.

TABLE I
Major Design Metrics for Recent Generations of Extreme Environment Durable SiC JFET-R ICs

	Gen. 10	**Gen. 11**	**Gen. 12**	**Gen. 13**
Gate Length	6 µm	6 µm	3 µm	3 µm
Res. Width	6 µm	3 µm	2 µm	1 µm
Contact Via	6 µm	6 µm	3 µm	2 µm
JFETs/Chip	~ 200	~ 1000	~ 3000	~ 10000
Die Width	3 mm	4.65 mm	5 mm	5 mm
Year	2017	2019	2022*	2023

* Delayed by prolonged COVID-19 NASA Glenn lab closure.

With modest adjustments, the SiC JFET-R fabrication process is compatible with semiconductor mass-production tools and materials. A separate paper at this conference will describe key issues to be addressed in transferring the SiC JFET-R IC process to semiconductor foundry manufacturing [6]. Towards this end, the processing that forms the SiC JFETs and resistors (without interconnect) for the IC Gen. 12 prototype IC run was recently competitively outsourced [15]. However, completion of the IC Gen. 12 fabrication run has been postponed by prolonged closure of the NASA Glenn SiC microfabrication laboratory arising from the COVID-19 pandemic.

Since accessibility and commercialization are key to technology infusion, NASA Glenn has entered formal partnerships to prototype limited numbers of developmental SiC JFET-R IC chips. Likewise, basic device/circuit models and mask layout design guidelines were publicly posted [16] and a basic device process development kit (PDK) was implemented for the design phase of the NASA Glenn JFET-R IC Gen. 12 wafer run. Potential users can thus explore circuit capabilities and possible benefits via design and simulation of their own application-specific JFET-R ICs. SiC JFET-R IC design services are also commercially available [17]. Under negotiated technology transfer and licensing agreements, a number of outside-user device designs have been prototyped in NASA Glenn SiC JFET-R wafers starting with IC Gen. 11. The next opportunity for prospective users to have devices fabricated on NASA Glenn developmental wafers will be the IC Gen. 13 SiC JFET-R prototype run slated to start in 2022. To facilitate substantial device shrinkage and corresponding chip complexity upscaling over Gen. 12 (as seen in Table I), stepper-based photolithography is planned for Gen. 13 IC fabrication. IC Gen. 13 calculated SPICE JFET and resistor device models and mask layout rules are posted online, and a basic Gen. 13 PDK will also become available in the near future [16].

Completing the SiC JFET-R electronics commercial design and production chain will lower investment and risk barriers to useful application deployment. Demonstrations of system benefits are also important. For NASA, an initial high-value deployment is opening the Venus surface to extended missions with greatly improved robotic scientific data return.

Enabling Infusion At NASA: Venus Landers

Long-term operation of silicon-based integrated circuits (ICs) has enabled a variety Mars lander missions to successfully operate in its cold (-143 °C to +27 °C) atmospheric environment returning valuably insightful scientific data for years. However, since Venus surface conditions fall well beyond the operating realm of silicon-based ICs, all prior Venus landers have employed high-mass pressure vessels and/or thermal insulation systems to protect mission-critical IC electronics from the ~ 460 °C, ~ 91 atm. pressure highly reactive atmospheric environment. Such protection measures have only worked for an hour or two before the surrounding Venus environment overcame the protection and thermally failed the silicon IC-based lander electronics. To date, the longest duration of data return from the surface of Venus surface is 2 hours and 7 minutes in 1978 by the ~760 kg Venera 13 lander [18,19]. A number of updated Venus lander designs relying on sheltered electronics have been studied over the intervening decades, including combinations of active cooling (refrigerator) subsystems and expanded silicon-IC capabilities. None of these sheltered-electronics approaches have increased surface science duration beyond a single day, and none have come in at less than 500 kg mass [18,19]. *The historical consequence of these severe drawbacks has been that no landers have touched down on the surface of Venus in over three decades, despite the widely recognized high scientific value of obtaining more comprehensive observations from the surface of Venus.*

Fig. 5. Comparison of proposed NASA Venus lander designs based upon sheltered electronics (left, [18]) versus unsheltered SiC electronics (right, [20]).

The proven ability of NASA Glenn SiC JFET-R ICs to function for 60 days immersed in the Venus surface environment without sheltering [11] offers sea-change improvements to Venus surface missions and scientific understanding. Based upon this realization, NASA has now initiated development of paradigm-shifting Venus surface mission concepts and demonstration hardware. One example of such a mission concept is the ~ 10 kg Long-Lived (or Long-Life) In-Situ Solar System Explorer (LLISSE) lander designed to return Venus surface meteorological data (including temperature, pressure, wind, and concentrations of selected atmospheric gasses) for more than 60 days [20]. Another example based on the same fundamental approach but with emphasis on seismology is the Seismic and Atmospheric Exploration of Venus (SAEVe) lander [21]. *By eliminating the need to protect its electronics from the Venus surface environment, the LLISSE and SAEVe concepts promise the order of 50-fold improvements in both mission duration and lander mass compared to designs that rely on environmentally sheltered electronics.* To complete such landers, sensors, energy storage (batteries), antennas, mechanical structure, etc. that are simultaneously low-mass, compact, and can effectively function for months immersed in the Venus surface environment without any cooling are undergoing parallel development along with mission-specific SiC JFET-R ICs. Landings on Venus are anticipated following long-term proofs of completely functional prototype landers in Venus atmospheric test chambers [22].

Summary

With the recent advancements in SiC JFET-R IC technology summarized in this paper, beneficial long-term IC deployment into previously unreachable extreme application environments is becoming enabled. This uniquely durable technology chain, starting from commercial SiC epiwafers through ceramic multi-chip circuit boards, can be realized via

modest modifications to standard IC design and mass-production practices and tooling. Further maturation and upscaling of this new capability is expected to take place in parallel with initial infusion deployments and transition to commercial manufacturing.

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Acronyms

ASIC: Application Specific Integrated Circuit
BJT: Bipolar Junction Transistor
GE: General Electric
GND: Ground
HTCC: High Temperature Co-fired Ceramic
IC: Integrated Circuit
IrIS: Iridium Interfacial Stack
JFET: Junction Field Effect Transistor
JFET-R: Junction Field Effect Transistor & Resistor
LET: Linear Energy Transfer
LLISSE: Long-Lived (or Long-Life) In-Situ Solar System Explorer
MOSFET: Metal Oxide Semiconductor Field Effect Transistor
NASA: National Aeronautics and Space Administration
PDK: Process Development Kit
SAEVe: Seismic and Atmospheric Exploration of Venus
SiC: Silicon Carbide
SOI: Silicon On Insulator
T: Temperature
TID: Total Ionizing Dose
V_T: JFET Threshold Voltage